

Abstract of the Disclosure

A clock generator comprising a master delay locked loop (DLL) and a slave DLL to capture a data signal. The slave DLL generates a slave output signal based on a clock signal. The master DLL receives the slave output signal and compensates variations in
5 delays of the data and clock signals to generate a capture clock signal. When the master and slave DLLs are locked, the capture clock signal is center aligned with the data signal.

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